DATA SHEET

L 65664

8 K x 8 / 3.3 VOLTS ULTIMATE CMOS SRAM

FEATURES

- **SINGLE SUPPLY 3.3 ± 0.3 VOLTS**
- **ACCESS TIME**
  COMMERCIAL : 55*/70/85 ns (max)
  MILITARY/INDUSTRIAL : 70*/75/85 ns (max)
- **VERY LOW POWER CONSUMPTION**
  ACTIVE : 105 mW (typ)
  STANDBY : 0.3 µW (typ)
  DATA RETENTION : 0.2 µW (typ)
- **WIDE TEMPERATURE RANGE :**
  - 55 °C TO + 125 °C
- **ASYNCHRONOUS**
- **EQUAL CYCLE AND ACCESS TIME**
- **GATED INPUTS : NO PULL-UP/DOWN RESISTORS ARE REQUIRED**

* Preliminary.

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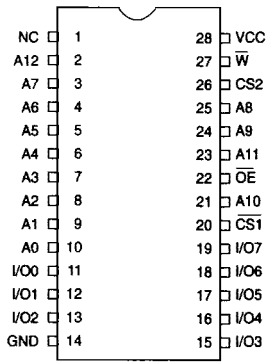
INTRODUCTION

The L65664 is a very low power CMOS static RAM organized as 8192 × 8 bits. It is manufactured using the MHS high performance SCMOS technology.
The L65664 provides fast access time of 55 ns for a 3 Volts power supply.
Utilising an array of six transistors (6T) memory cells, the L 65664 combines an extremely low standby supply current (typical value = 0.1 µA) with a fast access time of 55 ns. The high stability of the 6T cell provides excellent protection against soft errors due to noise.
Extra protection against heavy ions is given by the use of an epitaxial layer on a P substrate.
The L65664 is processed following the test methods of MIL STD 883C.

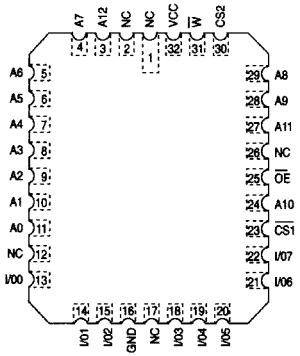
INTERFACE

PIN CONFIGURATION

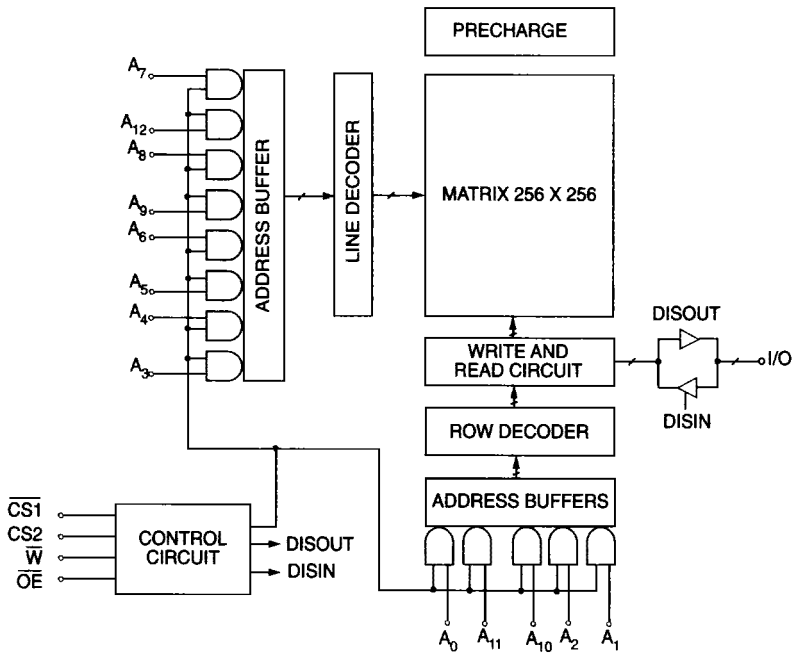
Pinout DIL/SO 28 pins (top view)



Pinout LCC 32 pins (top view)



BLOCK DIAGRAM



PIN DESCRIPTION

A0-A12	: Address inputs	$\overline{CS1}$	: Chip-select 1
I/O0-I/O7	: Input/Output	CS2	: Chip-select 2
Vcc	: Power	$\overline{OE}$	: Output Enable
Gnd	: Ground	$\overline{W}$	: Write enable

TRUTH TABLE

$\overline{CS1}$	CS2	$\overline{OE}$	$\overline{W}$	DATA-IN	DATA-OUT	MODE
H	X	X	X	Z	Z	Deselect
L	H	L	H	Z	Valid	Read
L	H	X	L	Valid	Z	Write
L	H	H	H	Z	Z	Output disable

L = low, H = high, X = H or L, Z = high impedance.

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply voltage to GND potential : - 0.5 V to + 7.0 V
Input or Output voltage applied : (Gnd - 0.3 V) to (Vcc + 0.3 V)
Storage temperature : - 65 °C to + 150 °C

OPERATING RANGE

	OPERATING VOLTAGE	OPERATING TEMPERATURE
Military	3.3 V ± 0.3 V	– 55 °C to + 125 °C
Industrial	3.3 V ± 0.3 V	– 40 °C to 85 °C
Commercial	3.3 V ± 0.3 V	0 °C to + 70 °C

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DC OPERATING CONDITIONS

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Vcc		Supply voltage	3	3.3	3.6	V
Gnd		Ground	0.0	0.0	0.0	V
VIL	(1)	Input low voltage	– 0.3	0.0	0.6	V
VIH		Input high voltage	1.8	–	Vcc + 0.3 V	V

Note : 1. VIL min = – 0.3 V or – 1.0 V pulse width 50 ns.

ELECTRICAL CHARACTERISTICS DC PARAMETER

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
IIX	(2)	Input leakage current	– 1.0	–	1	µA
IOZ	(2)	Output leakage current	– 1.0	–	1.0	µA
VOL	(3)	Output low voltage	–	–	0.4	V
VOH	(3)	Output high voltage	2	–	–	V

Notes : 2. Gnd < Vin < Vcc, Gnd < Vout < Vcc Output disabled.
3. Vcc min, IOL = 1 mA, IOH = – 0.5 mA.

CAPACITANCE

PARAMETER		DESCRIPTION	MINIMUM	TYPICAL	MAXIMUM	UNIT
Cin	(4)	Input capacitance	–	–	8	pF
Cout	(4)	Output capacitance	–	–	8	pF

Note : 4. TA = 25 °C, f = 1 MHz, Vcc = 5.0 V, these parameters are not tested.

CONSUMPTION FOR COMMERCIAL SPECIFICATION

SYMBOL	PARAMETER	L 65664 V-55	L 65664 L-55	L 65664 V-70	L 65664 L-70	L 65664 V-85	L 65664 L-85	UNIT	VALUE
ICCSB (5)	Standby supply current	5	10	5	10	5	10	mA	max
ICCSB1 (6)	Standby supply current	0.7	40	0.7	40	0.7	40	µA	max
ICCOP (7)	Operating supply current	50	70	50	70	50	70	mA	max

CONSUMPTION FOR INDUSTRIAL SPECIFICATION

SYMBOL	PARAMETER	L 65664 V-70	L 65664 L-70	L 65664 V-75	L 65664 L-75	L 65664 V-85	L 65664 L-85	UNIT	VALUE
ICCSB (5)	Standby supply current	10	15	10	15	10	15	mA	max
ICCSB1 (6)	Standby supply current	3	50	3	50	3	50	µA	max
ICCOP (7)	Operating supply current	55	75	55	75	55	75	mA	max

CONSUMPTION FOR MILITARY SPECIFICATION

SYMBOL	PARAMETER	L 65664 V-70	L 65664 L-70	L 65664 V-75	L 65664 L-75	L 65664 V-85	L 65664 L-85	UNIT	VALUE
ICCSB (5)	Standby supply current	10	15	10	15	10	15	mA	max
ICCSB1 (6)	Standby supply current	30	300	30	300	30	300	µA	max
ICCOP (7)	Operating supply current	55	75	55	75	55	75	mA	max

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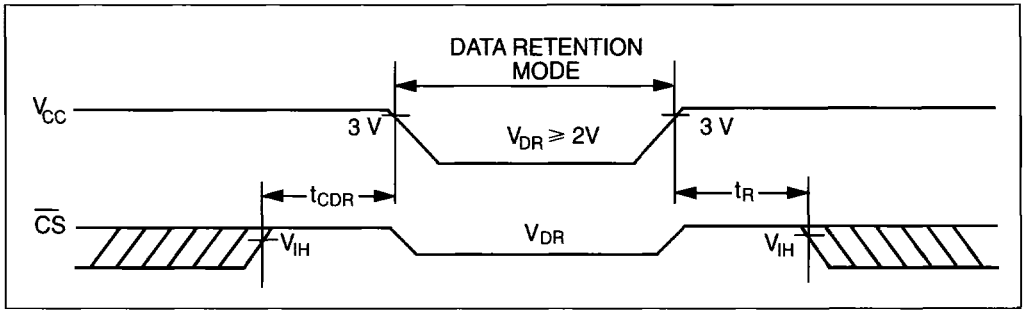
Notes : 5. $\overline{CS1} \geq VIH$, $CS2 \leq VIL$, $Vin \geq VIH$ or $Vin \leq VIL$.
6. $\overline{CS1} \geq Vcc - 0.3$ V, $CS2 \leq 0.3$ V, Iout = 0 mA. $Vin \geq Vcc - 0.3$ V or $Vin \leq 0.3$ V.
7. Vcc max, Iout = 0 mA, f = max, Vin = Gnd/Vcc.
"For Low frequency application consult us."

DATA RETENTION MODE

MHS CMOS RAM's are designed with battery backup applications in mind. Data retention voltage and supply current are guaranteed over temperature. The following rules insure data retention :

1. Chip select ($\overline{CS}$) must be held high during data retention ; within Vcc to Vcc – 0.2 V.
2. Output Enable ($\overline{OE}$) should be held high to keep the RAM outputs high impedance, minimizing power dissipation.
3. $\overline{CS}$ and $\overline{OE}$ must be kept between Vcc + 0.3 V and 70 % of Vcc during the power up and power down transitions.
4. The RAM can begIn operation > 55 ns after Vcc reaches the minimum operating voltage (3 V).

TIMING



DATA RETENTION CHARACTERISTICS

PARAMETER	DESCRIPTION	MINIMUM	TYPICAL (8)				UNIT
VCCDR	Vcc for data retention	2.0	–	–			V
TCDR	Chip deselect to data retention time	0.0	–	–			ns
TR	Operation recovery time	TAVAV (9)	–	–			ns
ICCDR1 (10)	Data retention current			COM	IND	MIL	
	@ 2.0 V : L-65664V-55	–	0.1	0.5	–	–	µA
	L-65664L-55	–	0.1	30	–	–	µA
	L-65664V-70/75/85	–	0.1	0.5	2	20	µA
	L-65664L-70/75/85	–	0.1	30	40	200	µA

Notes : 8. TA = 25 °C
9. TAVAV = Read cycle time.
10. $\overline{CS}$ = Vcc, Vin = Gnd/Vcc.

AC PARAMETERS

AC CONDITIONS :

Input pulse levels : Gnd to 3.0 V
Input rise : 5 ns
Input timing reference levels : 1.2 V
Output load : See fig. 1a, 1b

AC TEST LOADS AND WAVEFORMS

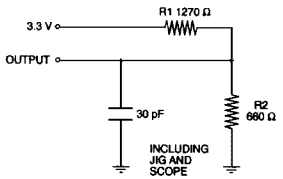


Figure 1 a

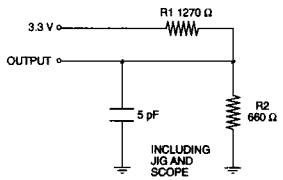


Figure 1 b

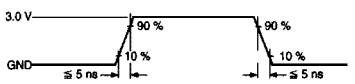
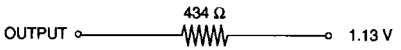


Figure 2

Equivalent to : THEVENIN EQUIVALENT



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WRITE CYCLE : COMMERCIAL SPECIFICATION (note 12)

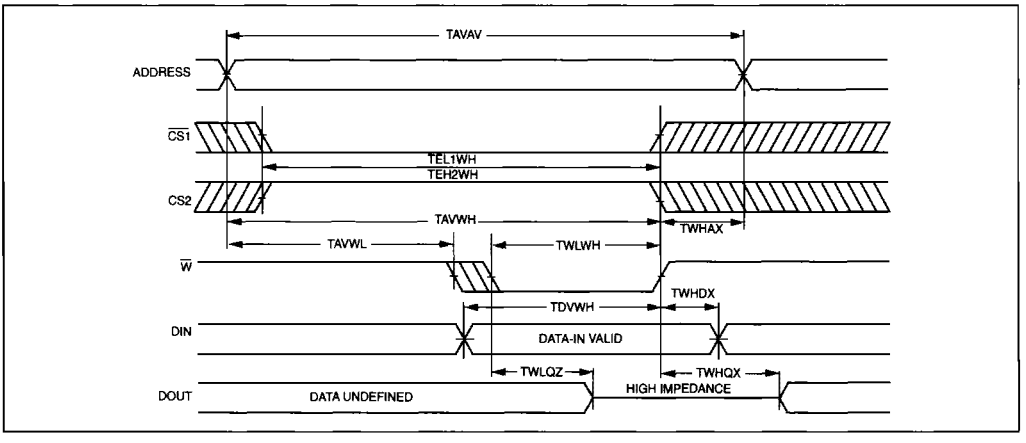
SYMBOL	PARAMETER	L 65664 V-55	L 65664 L-55	L 65664 V-70	L 65664 L-70	L 65664 V-85	L 65664 L-85	UNIT	VALUE
TAVAV	Write cycle time	55	55	70	70	85	85	ns	min
TAVWL	Address set-up time	0	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	50	50	60	60	75	75	ns	min
TDVWH	Data set-up time	35	35	45	45	55	55	ns	min
TEL1WH	$\overline{CS1}$ low to write end	50	50	60	60	75	75	ns	min
TEH2WH	CS2 low to write end	50	50	60	60	75	75	ns	min
TWLQZ (11)	Write low to high Z	25	25	25	25	30	30	ns	max
TWLWH	Write pulse width	50	50	65	65	80	80	ns	min
TWHAX	Address hold to end of write	2	2	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	0	0	0	ns	min

WRITE CYCLE : INDUSTRIAL AND MILITARY SPECIFICATION (note 12)

SYMBOL	PARAMETER	L 65664 V-70	L 65664 L-70	L 65664 V-75	L 65664 L-75	L 65664 V-85	L 65664 L-85	UNIT	VALUE
TAVAV	Write cycle time	70	70	75	75	85	85	ns	min
TAVWL	Address set-up time	0	0	0	0	0	0	ns	min
TAVWH	Address valid to end of write	60	60	65	65	75	75	ns	min
TDVWH	Data set-up time	45	45	50	50	55	55	ns	min
TEL1WH	$\overline{CS1}$ low to write end	60	60	65	65	75	75	ns	min
TEH2WH	CS2 low to write end	60	60	65	65	75	75	ns	min
TWLQZ (11)	Write low to high Z	25	25	25	25	30	30	ns	max
TWLWH	Write pulse width	65	65	70	70	80	80	ns	min
TWHAX	Address hold to end of write	2	2	2	2	2	2	ns	min
TWHDX	Data hold time	0	0	0	0	0	0	ns	min
TWHQX (11)	Write high to low Z	0	0	0	0	0	0	ns	min

Note : 11. Specified with C_L = 5 pF (see figure 1b). Guaranteed. Not tested.

WRITE CYCLE : 1 $\overline{W}$ CONTROLLED (note 12)



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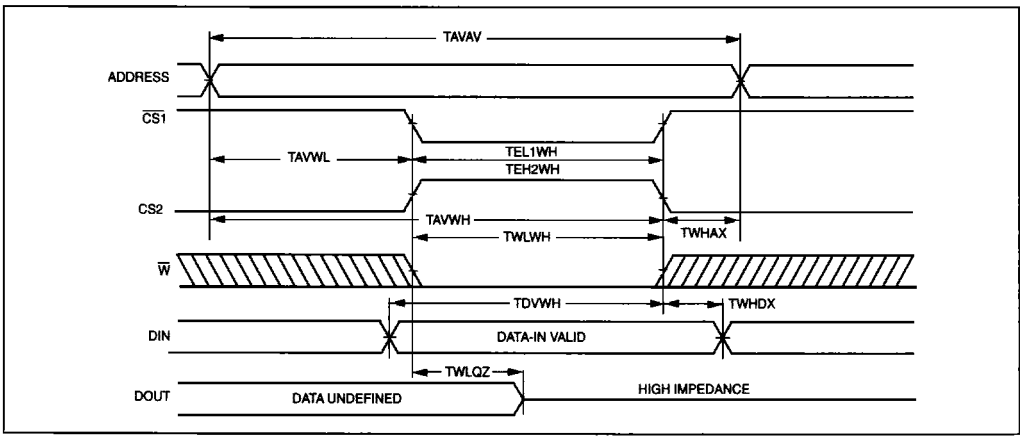
WRITE CYCLE : 2 $\overline{CS1}$ CONTROLLED (note 12)



Note : 12. The internal write time of the memory is defined by the overlap of $\overline{CS}$ LOW and $\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
Data out is high impedance if $\overline{OE}$ = VIH.

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READ CYCLE : COMMERCIAL SPECIFICATION

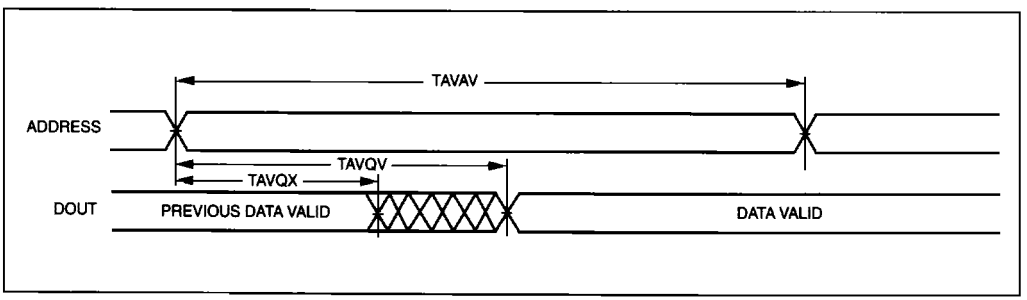
SYMBOL	PARAMETER	L 65664 V-55	L 65664 L-55	L 65664 V-70	L 65664 L-70	L 65664 V-85	L 65664 L-85	UNIT	VALUE
TAVAV	Write cycle time	55	55	70	70	85	85	ns	min
TAVQV	Address access time	55	55	70	70	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	55	55	70	70	85	85	ns	max
TEH2QV	Chip-select 2 access time	55	55	70	70	85	85	ns	max
TEL1QX (13)	$\overline{CS1}$ low to low Z	5	5	5	5	5	5	ns	min
TEH2QX (13)	CS2 to low Z	5	5	5	5	5	5	ns	min
TEH1QZ (13)	$\overline{CS1}$ high to high Z	35	35	45	45	55	55	ns	max
TEL2QZ (13)	CS2 low to high Z	35	35	45	45	55	55	ns	max
TGLQV	Output Enable access time	25	25	30	30	40	40	ns	max
TGLQX (13)	$\overline{OE}$ low to low Z	5	5	5	5	5	5	ns	min
TGHQZ (13)	$\overline{OE}$ high to high Z	25	25	30	30	40	40	ns	max

READ CYCLE : INDUSTRIAL AND MILITARY SPECIFICATION

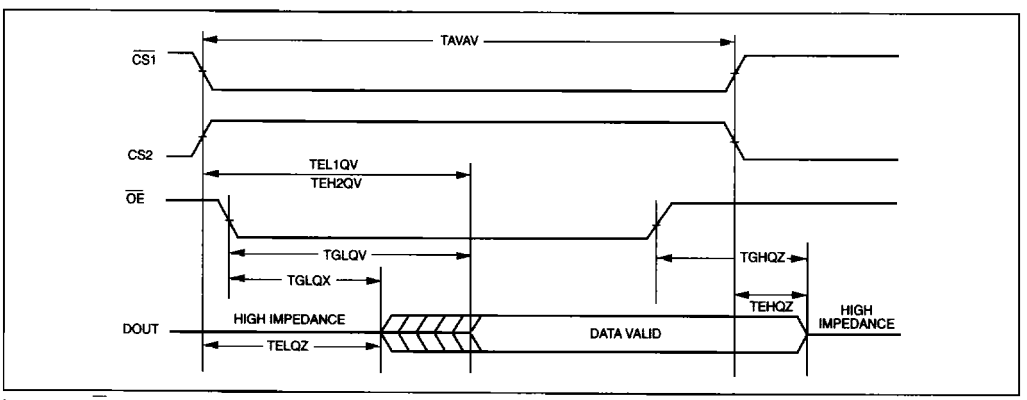
SYMBOL	PARAMETER	L 65664 V-70	L 65664 L-70	L 65664 V-75	L 65664 L-75	L 65664 V-85	L 65664 L-85	UNIT	VALUE
TAVAV	Read cycle time	70	70	75	75	85	85	ns	min
TAVQV	Address access time	70	70	75	75	85	85	ns	max
TAVQX	Address valid to low Z	5	5	5	5	5	5	ns	min
TEL1QV	Chip-select 1 access time	70	70	75	75	85	85	ns	max
TEH2QV	Chip-select 2 access time	70	70	75	75	85	85	ns	max
TEL1QX (13)	$\overline{CS1}$ low to low Z	5	5	5	5	5	5	ns	min
TEH2QX (13)	CS2 high to low Z	5	5	5	5	5	5	ns	min
TEH1QZ (13)	$\overline{CS1}$ high to high Z	45	45	45	45	55	55	ns	max
TEL2QZ (13)	CS2 low to high Z	45	45	45	45	55	55	ns	max
TGLQV	Output Enable access time	30	30	35	35	40	40	ns	max
TGLQX (13)	$\overline{OE}$ low to low Z	5	5	5	5	5	5	ns	min
TGHQZ (13)	$\overline{OE}$ high to high Z	30	30	35	35	40	40	ns	max

Note : 13. Guaranteed but not tested.

READ CYCLE nb 1 (notes 14, 15)

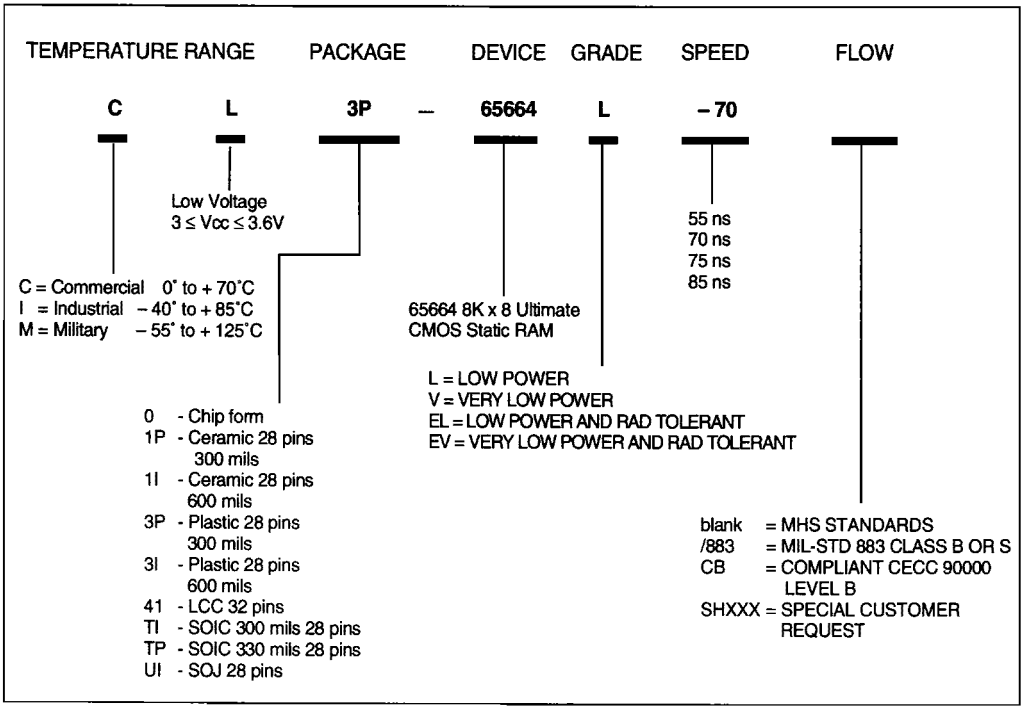


READ CYCLE nb 2 (notes 14, 16)



Notes : 14. $\overline{W}$ is high for read cycle.
15. Device is continuously selected, $\overline{CS1}$ & $\overline{OE}$ = VIL and CS2 = VIH.
16. Address valid prior to or coincident with CS transition low.

ORDERING INFORMATION



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